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10/064,777	08/16/2002	Hsin-Ta Lee	CMOP0023USA	2572

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EXAMINER	
LABAZE, EDWYN	
ART UNIT	PAPER NUMBER
2876	

DATE MAILED: 10/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Applicati n N .	Applicant(s)
	10/064,777	LEE ET AL.
	Examiner	Art Unit
	EDWYN LABAZE	2876

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 August 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-43 are presented for examination.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-43 are rejected under 35 U.S.C. 102(b) as being anticipated by Hara et al. (U.S. 6,046,790).

Re claim 1: Hara et al. discloses LCD device having relationship between spontaneous polarization and capacitance, which includes an upper/first substrate 14 (col.22, lines 14+), a lower/second substrate 1 (col.22, lines 52+), and a plurality of pixels 11 located between the upper/first substrate 1 and the lower/second substrate 14, each of the pixels 11 having at least a compensating capacitor 26 for providing an approximately identical feed-through voltage for each of the pixels (See Fig. # 3 of Hara et al.; and col.19, lines 30-61; col.24, lines 42-67).

Re claims 2, 23: Hara et al. teaches an apparatus, further comprising a first scanning line, a second scanning line 2 (See Figs. # 1A, 2A of Hara et al.), and a scanning line driving circuit

21 (Figs. # 1A, 6A of Hara et al.; col.33, lines 19+), each of the pixels being located between the first scanning line and the second scanning line 2, each of the first scanning line and the second scanning line having a first input end so that the scanning line driving circuit can input signals into the first scanning line and the second scanning line through the first input ends (col.30, lines 5-67).

Re claim 3: Hara et al. discloses an apparatus, wherein a capacitance of each of the compensating capacitors is increased when a distance between the pixels and the first input end of the second scanning line [also known in the art as the spontaneous polarization, which is the capacitance per unit electrode area/distance of the liquid crystal] is increased (col.35, lines 50+; col.36, lines 44+).

Re claim 4: Hara et al. teaches an apparatus, wherein each of the pixels further comprises a liquid crystal cell A (See Fig. # 2a of Hara et al.) having a common electrode 16 (col.23, lines 50+), a pixel electrode 11 connected to the corresponding compensating capacitor 26 (Fig. # 3 of Hara et al.; col.24, lines 43+), and a liquid crystal layer disposed between the pixel electrode 11 and the common electrode 16 (col.11, lines 56+; col.18, lines 49-67 and col.43, lines 24+); and a thin film transistor or TFT having a gate electrode 2a connected to the first scanning line, a drain electrode 10b connected to a corresponding first data line, and a source electrode 10a connected to the pixel electrode 11 (col.12, lines 43+; col.25, lines 25-67).

Re claims 5, 13: Hara et al. teaches an apparatus, wherein each of the compensating capacitors is composed of a first overlapping region 32 which is formed by overlapping the corresponding pixel electrode 11 over the first scanning line 2 (col.25, lines 44-67).

Re claims 6, 14, 20: Hara et al. discloses an apparatus, wherein an area of each of the first overlapping regions is increased as a distance between the first input end of the first scanning line and the pixel corresponding to each of the first overlapping (col.23, lines 47-67; col.24, lines 55-67; col.32, lines 3-34).

Re claims 7, 15, 21: Hara et al. teaches an apparatus, wherein each of the compensating capacitors is composed of a second overlapping region or interlayer 34, which is formed by overlapping the corresponding source electrode 10a over the corresponding gate electrode 2a (col.26, lines 56-67).

Re claims 8, 16, 28, 29: Hara et al. discloses an apparatus, wherein an area of each of the second overlapping regions is increased as a distance between the first/second input end of the first scanning line and the pixel corresponding to each of the second overlapping regions is increased (col.31, lines 58-67; col.32, lines 1-35).

Re claims 9, 17: Hara et al. teaches an apparatus, wherein each of the pixels further comprises a storage capacitor 12 (col.23, lines 42+), and a capacitance of each of the storage capacitors is reduced as a distance between each of the storage capacitors 12 and the first input end of the second scanning line is increased (col.25, lines 5+).

Re claim 10: Hara et al. discloses an apparatus, further comprising a second data line and a data line driving circuit 21, each of the pixels being connected to the second data line, which has a second input end so that the data line driving circuit 21 can input signals into the second data line through the second input end (See Fig.# 1A of Hara et al., with more than one drive circuits).

Re claim 11: Hara et al. teaches an apparatus, wherein a capacitance of each of the compensating capacitors is increased as a distance between each of the compensating capacitors and the second input end [also known in the art as the spontaneous polarization, which is the capacitance per unit electrode area/distance of the liquid crystal] is increased (col.35, lines 50+; col.36, lines 44+).

Re claim 12: Hara et al. discloses an apparatus, wherein each of the pixels is located between a third scanning line and a fourth scanning line, and further comprises: a liquid crystal cell B (See Fig. # 2a of Hara et al.) having a common electrode 16 (col.23, lines 50+), a pixel electrode 11 connected to the corresponding compensating capacitor 26 (Fig. # 3 of Hara et al.; col.24, lines 43+), and a liquid crystal layer disposed between the pixel electrode 11 and the common electrode (col.11, lines 56+; col.18, lines 49-67 and col.43, lines 24+), and a thin film transistor/TFT having a gate electrode 2a to the corresponding third scanning line (See Fig. # 1 of Hara et al.), a drain electrode 10b connected to the second data line, and a source electrode 10a connected to the pixel electrode 11 (col.12, lines 43+; col.25, lines 25-67).

Re claim 18: Hara et al. teaches an apparatus, which includes a plurality of scanning or gate lines 2 (col.22, lines 15+); a plurality of data or signal lines 4 (as shown in Figs. # 1A, 6A, 7A, and 12 of Hara et al.; col.22, lines 16+); and a plurality of pixels, each of the pixels having a pixel electrode 11 (col.25, lines 50+), and a thin film transistor/TFT having a gate electrode 2a connected to the corresponding scanning line 2 (See Fig. # 1A of Hara et al.), a drain electrode 10b connected to the corresponding data line 4, and a source electrode 10a connected to the pixel electrode 11 (col.12, lines 43+; col.25, lines 25-67), wherein a first overlapping region/ interlayer 32 is formed by overlapping the pixel electrode 11 over the corresponding scanning line; wherein

an area of each of the first overlapping regions is increased gradually along a first direction (col.33, lines28-67; col.34, lines 1+) .

Re claim 19: Hara et al. discloses an apparatus, wherein each of the first overlapping region 32 forms a compensating capacitor for providing an approximately identical feed-through voltage for each of the pixels, thus reducing a flicker effect of the liquid crystal display panel (col.19, lines 30-61).

Re claim 22: Hara et al. discloses an apparatus, wherein a protrusion structure is disposed on each of the pixel electrodes 11 and above the corresponding second extending portion, for regulating an alignment direction of liquid crystal molecules (col.2, lines 22-67; col.3, lines 1-35).

Re claim 24: Hara et al. teaches an apparatus, wherein the first direction is parallel to each of the scanning/gate lines 2 (col.25, lines 25+), and an area of each of the first overlapping regions 32 is increased as a distance between each of the first overlapping regions or interlayer 32 and the first input end of the scanning line 2 corresponding to each of the first overlapping regions is increased (col.23, lines 47-67; col.24, lines 55-67; col.32, lines 3-34).

Re claim 25: Hara et al. discloses an apparatus, wherein the first direction is parallel to each of the data lines 4 (col.25, lines 25+), and an area (also disclosed as the disposition period, which is 200 microns as a result of the cross-section between the gate/scan line 300 microns and the data/signal line 100 microns; see col.39, lines 58+) of each of the first overlapping regions 32 is increased as a distance (which is the same for the interlayer region, since the length of each pixel is the same) between each of the first overlapping regions and the second input end of the data line 4 corresponding to each of the first overlapping regions is increased (col.32, lines 1-67).

Re claim 27: Hara et al. teaches an apparatus, wherein each of the second overlapping or interlayer regions 34 forms a compensating capacitor (two conductive elements separated by a non-conductive layer) for providing an approximately identical feed-through voltage for each of the pixels (col.26, lines 56-67), thus reducing a flicker effect of the liquid crystal display panel (col.19, lines 30-61).

Re claim 30: Hara et al. discloses an apparatus, comprising of a scanning line driving or gate circuit 21, at least a scanning/gate line 2 connected to the scanning line driving circuit 21 (fig. # 1A of Hara et al.; col.28, lines 16+), a first region A positioned on the scanning line 2 having at least a first pixel, which comprises a first pixel electrode 11 (col.23, lines 47+), a first overlapping or interlayer region 31 being formed by overlapping the first pixel electrode 11 over the scanning line 2 (col.25, lines 44+); and a second region positioned on the scanning line 2 having at least a second pixel, which comprises a second pixel electrode, a second overlapping region 32 being formed by overlapping the second pixel electrode 11 over the scanning line (col.25, lines 55+); wherein the first region is located between the scanning line driving circuit 21 and the second region, and an area of the second overlapping region is larger than an area of the first overlapping region (see figs. # 5B and 7B) .

Re claim 31: Hara et al. teaches an apparatus, wherein the first pixel further comprises a first thin film transistor/TFT, which includes a first gate electrode 2a connected to the scanning line 2, a first drain electrode 10b connected to a first data line, and a first source electrode 10a connected to the first pixel electrode 11, and a third overlapping region is formed by overlapping the first source electrode 10a over the first gate electrode 2a (see Fig. # 5B of Hara et al.).

Re claim 32: Hara et al. discloses an apparatus, wherein the second pixel further comprises a second thin film transistor, which includes a second gate electrode [same as first gate electrode, but for a different pixel] 2a connected to the scanning line 2, a second drain electrode 10b connected to a second data line 2, and a second source electrode 10a connected to the second pixel electrode 11, and a fourth overlapping region 34 is formed by overlapping the second source electrode 10a over the second gate electrode 2a (col.26, lines 56+).

Re claim 33: Hara et al. teaches an apparatus, wherein an area of the fourth overlapping region [which is the same as interlayer region 34, but for a different pixel] is larger than an area of the third overlapping [same as interlayer 32] region (see Fig. # 5B of Hara et al.).

Re claim 34: Hara et al. teaches an apparatus, a data/signal line driving circuit 22, at least a data/signal line 4 connected to the data line driving circuit 22 (col.28, lines 1-20); a first region positioned on the data line having at least a first thin film transistor (see fig. # 1A of Hara et al.), which comprises a first gate electrode 2a connected to a first scanning/gate line 2, a first drain electrode 10b connected to the data/signal line 4 (col.22, lines 34+), and a first source electrode 10a connected to a first pixel electrode 11, a first overlapping/interlayer region 31 being formed by overlapping the first pixel electrode 11 over the first scanning line 2 (col.25, lines 44+); and a second region positioned on the data line having at least a second thin film transistor, which comprises a second gate electrode 2a [same as first gate electrode, but for a different pixel] connected to a second scanning line 2 , a second drain electrode 10b connected to the data/signal line 4, and a second source electrode 10a connected to a second pixel electrode [same as the first pixel] 11, a second overlapping/interlayer region 34 being formed by overlapping the second pixel electrode 11 over the second scanning line (col26, lines 56+); wherein the first region is

located between the data line driving circuit 22 and the second region, and an area of the second overlapping region 34 is larger than an area of the first overlapping region 31 (see figs. # 5B and 7B).

Re claim 35: Hara et al. discloses an apparatus, wherein a third overlapping region [same as the first interlayer region 31] is formed by overlapping the first source electrode 10a over the first gate electrode 2a, a fourth overlapping region is formed by overlapping the second source electrode over the second gate electrode, and an area of the fourth overlapping region 34 [same as the second interlayer, but different pixel] is larger than an area of the third overlapping region 31 (see figs. # 5B and 7B).

Re claim 36: Hara et al. teaches an apparatus, wherein the first region comprises a plurality of first thin film transistors, and an area of each of the first overlapping regions 31 is increased as a distance between the data/signal line driving circuit 22 and the first thin film transistor corresponding to each of the first overlapping regions is increased (col.36, lines 57+).

Re claim 37: Hara et al. discloses an apparatus, wherein the second region comprises a plurality of second thin film transistors, and an area of each of the second overlapping regions 32 is increased as a distance between the data/signal line driving circuit 22 and the second thin film transistor corresponding to each of the second overlapping regions 32 is increased (col.25, lines 50-67; col.26, lines 1-27).

Re claim 38: Hara et al. teaches an apparatus, which includes a plurality of scanning lines 2 for transmitting scanning signals from a scanning or gate line driving circuit 21 (fig. # 1A, 6A, of Hara et al.; col.22, lines 64+), a plurality of data/signal lines 4 for transmitting image signals from a data/signal line driving circuit 22 (col.22, lines 63+); and a plurality of pixels 11, each of

the pixels comprising a liquid crystal capacitor/cell 23 (see Fig. # 3 of Hara et al. col.24, lines 42+), a thin film transistor/TFT electrically connected to the corresponding scanning line 2, the corresponding data/signal line 4, and the liquid crystal capacitor/cell 23, and a compensating capacitor 26 electrically connected between the liquid crystal capacitor 23 and the corresponding scanning line, being connected to the thin film transistor/TFT, for providing an approximately identical feed-through voltage for each of the pixels (See Fig. # 3 of Hara et al.; and col.19, lines 30-61; col.24, lines 42-67).

Re claim 39: Hara et al. discloses an apparatus, wherein a capacitance of each of the compensating capacitors is increased as a distance between each of the pixels and the scanning or gate line driving circuit 21 is increased (col.13, lines 1-67; col.14, lines 1+).

Re claim 40: Hara et al. teaches an apparatus, wherein a capacitance of each of the compensating capacitors is increased as a distance between each of the pixels and the data/signal line driving circuit 22 is increased (col.13, lines 1-67; col.14, lines 1+).

Re claim 41: Hara et al. discloses an apparatus, further comprising a storage capacitor 12 connected to the liquid crystal capacitor/cell (see fig. # 3 of Hara et al.; col.24, lines 42+).

Re claim 42: Hara et al. teaches an apparatus, wherein a capacitance of each of the storage capacitors 12 is reduced as a distance between each of the storage capacitors and the scanning line driving circuit 21 is increased (col.13, lines 50-67; col.14, lines 1-67).

Re claim 43: Hara et al. discloses an apparatus, wherein a capacitance of each of the storage capacitors 12 is reduced as a distance between each of the storage capacitors and the data line driving circuit 22 is increased (col.13, lines 50-67; col.14, lines 1-67).

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Suzuki et al. (U.S. 5,235,448) discloses liquid crystal display having proportional TFT channel width.

Kambara et al. (U.S. 5,629,783) teaches active matrix polymer dispersed liquid crystal display device with fluorescent film.

Nakashima et al. (U.S. 5,745,194) discloses active matrix LCD with compensating capacitor having a particular feature.

Kouchi et al. (U.S. 5,886,365) teaches liquid crystal display device having a capacitor in the peripheral driving circuit.

Ohta et al. (U.S. 5,978,059) discloses liquid crystal display device with wide viewing angle characteristics.

Kuroha et al. (U.S. 6,028,650) teaches liquid crystal display apparatus with uniform feed-through voltage in panel.

Okumura et al. (U.S. 6,115,018) discloses active matrix liquid crystal display device.

Yeo et al. (US 2002/0080317) teaches liquid crystal display device and method for fabricating the same.

Sasaki (JP 04225329) discloses active matrix liquid crystal display.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to EDWYN LABAZE whose telephone number is (703) 305-5437. The examiner can normally be reached on 7:30 AM - 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael G. Lee can be reached on (703) 305-3503. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

el
Edwyn Labaze
Patent Examiner
Art Unit 2876
September 27, 2003

Karl D. Frech

KARL D. FRECH
PRIMARY EXAMINER